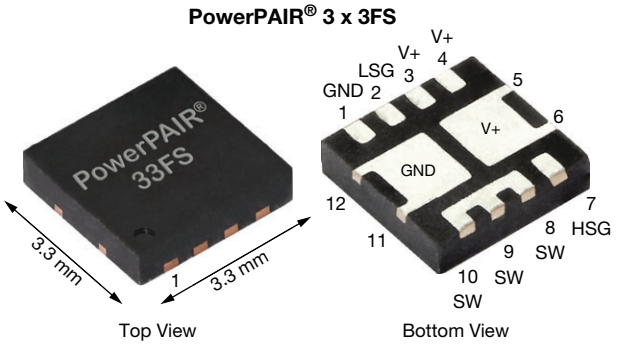
Dual N-Channel 30 V (D-S) MOSFET

PowerPAIR® 3 x 3FS



FEATURES

- TrenchFET® Gen V power MOSFET
- Symmetric dual N-channel
- Flip chip technology optimal thermal design
- High side and low side MOSFETs form optimized combination for 50 % duty cycle
- Optimized R_{DS} - Q_g and R_{DS} - Q_{gd} FOM elevates efficiency for high frequency switching
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

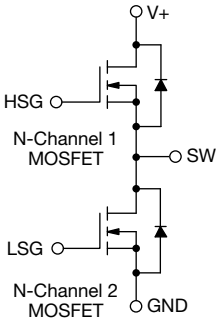
RoHS COMPLIANT
HALOGEN FREE

PRODUCT SUMMARY

V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.0032
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.0053
Q_g typ. (nC)	6.7
I_D (A)	100 [a]
Configuration	Dual

APPLICATIONS

- Synchronous buck
- Computer / server peripherals
- Half bridge
- POL
- Telecom DC/DC



ORDERING INFORMATION

Package	PowerPAIR 3 x 3FS
Lead (Pb)-free and halogen-free	SiZF5302DT-T1-RE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	+16 / -12	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	100	A
	T_C = 70 °C		80	
	T_A = 25 °C		28.1 [b, c]	
	T_A = 70 °C		22.5 [b, c]	
Pulsed drain current (t = 100 µs)		I_{DM}	150	
Continuous source current (MOSFET diode conduction)	T_C = 25 °C	I_S	40.1	
	T_A = 25 °C		3.2 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	17	
Single pulse avalanche energy		E_{AS}	14.45	mJ
Maximum power dissipation	T_C = 25 °C	P_D	48.1	W
	T_C = 70 °C		30.8	
	T_A = 25 °C		3.8 [b, c]	
	T_A = 70 °C		2.4 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature)			260	

Notes

a. T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s

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THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [a, b]	t ≤ 10 s	R_{thJA}	26	33	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	2	2.6	

Notes

a. Surface mounted on 1" x 1" FR4 board

b. Maximum under steady state conditions is 67 °C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 1 mA	30	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1	-	2	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +16 V / -12 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55 °C	-	-	5	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	30	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	-	0.0027	0.0032	Ω
		V_{GS} = 4.5 V, I_D = 7 A	-	0.0044	0.0053	
Forward transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 10 A	-	57	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	-	1030	-	pF
Output capacitance	C_{oss}		-	340	-	
Reverse transfer capacitance	C_{rss}		-	30	-	
C_{rss}/C_{iss} ratio			-	0.028	0.055	
Total gate charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 20 A	-	14.8	22.2	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A	-	6.7	10.0	
Gate-source charge	Q_{gs}		-	3.8	-	
Gate-drain charge	Q_{gd}		-	1.12	-	
Gate resistance	R_g	f = 1 MHz	0.24	1.2	2.4	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1 Ω, I_D ≅ 15 A, V_{GEN} = 10 V, R_g = 1 Ω	-	10	20	ns
Rise time	t_r		-	6	12	
Turn-off delay time	$t_{d(off)}$		-	23	46	
Fall time	t_f		-	6	12	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1 Ω, I_D ≅ 15 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	20	40	
Rise time	t_r		-	45	90	
Turn-off delay time	$t_{d(off)}$		-	20	40	
Fall time	t_f		-	12	24	
Drain-source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25°C	-	-	40.1	A
Pulse diode forward current	I_{SM}		-	-	150	
Body diode voltage	V_{SD}	I_S = 15 A, V_{GS} = 0 V	-	0.85	1.2	V
Body diode reverse recovery time	t_{rr}	I_F = 15 A, di/dt = 100 A/µs, T_J = 25 °C	-	13	26	ns
Body diode reverse recovery charge	Q_{rr}		-	3	6	nC
Reverse recovery fall time	t_a		-	6	-	ns
Reverse recovery rise time	t_b		-	7	-	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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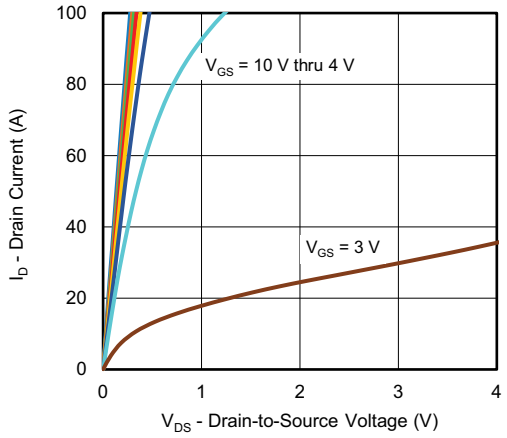
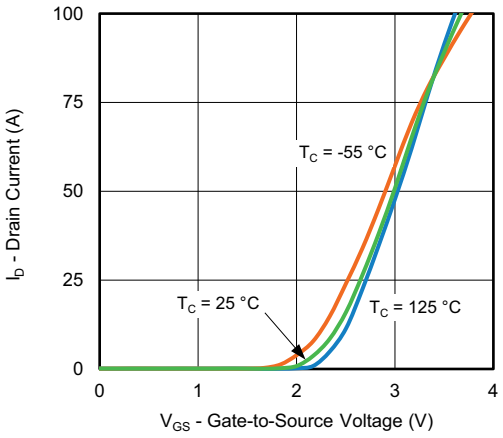
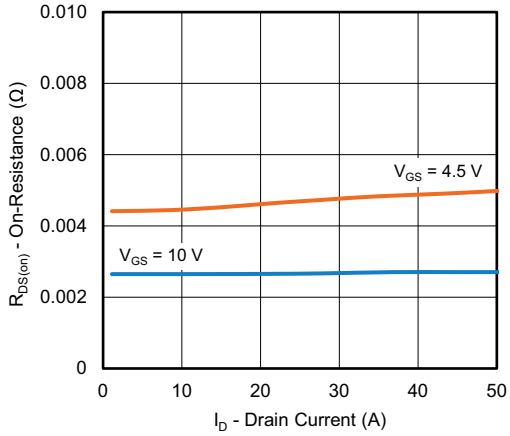


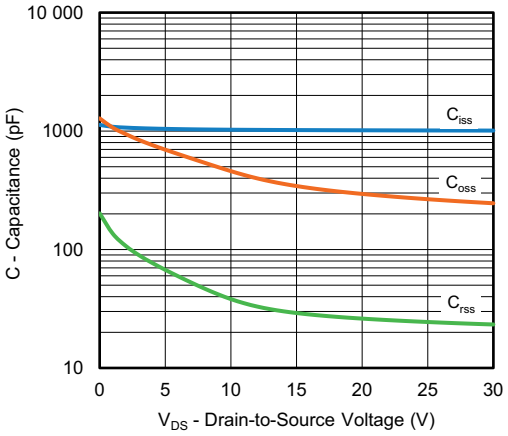
Output Characteristics



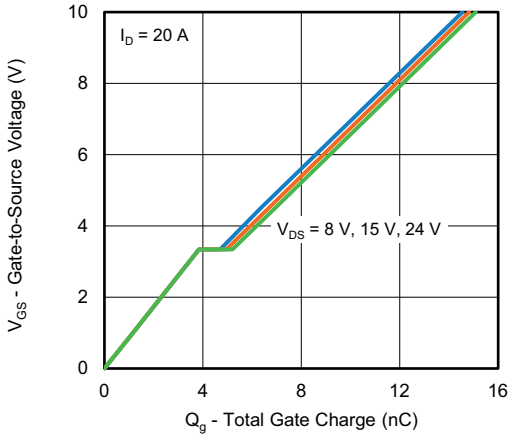
Transfer Characteristics



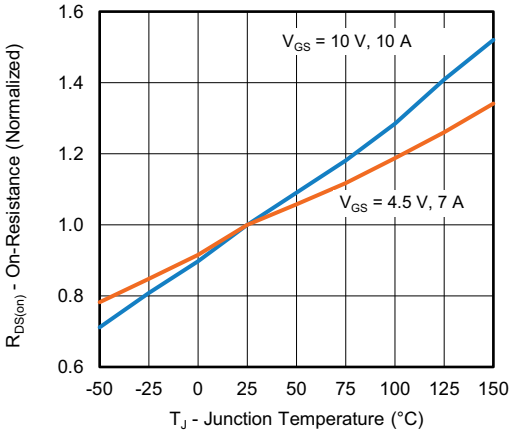
On-Resistance vs. Drain Current and Gate



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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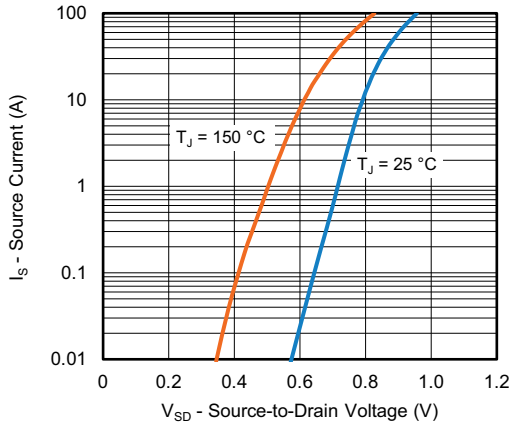
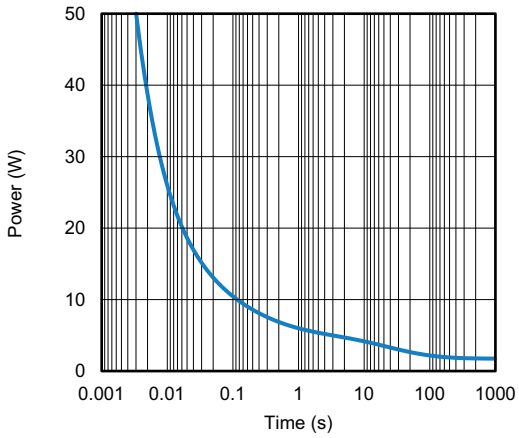
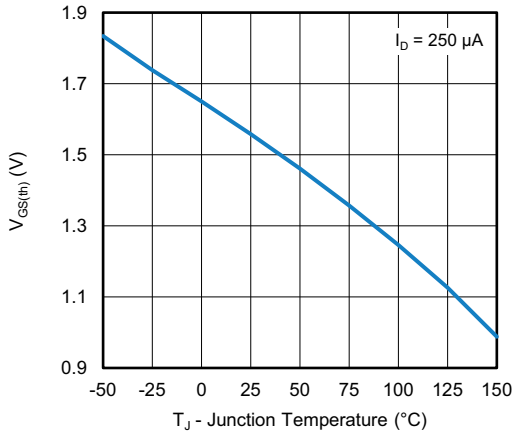


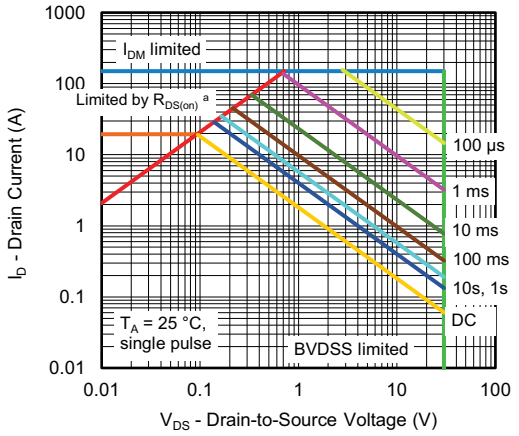
Source-Drain Diode Forward Voltage



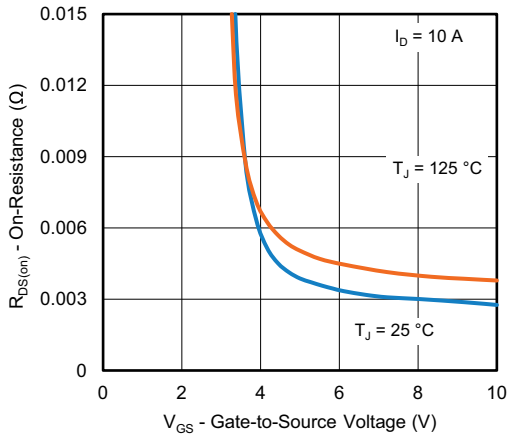
Single Pulse Power



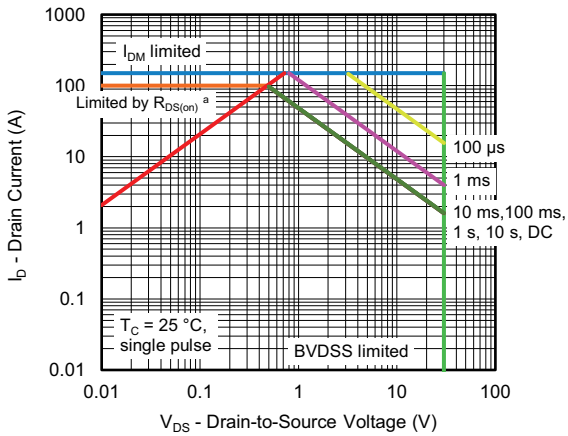
Threshold Voltage



Safe Operating Area, Junction-to-Ambient



On-Resistance vs. Gate-to-Source Voltage



Safe Operating Area, Junction-to-Case

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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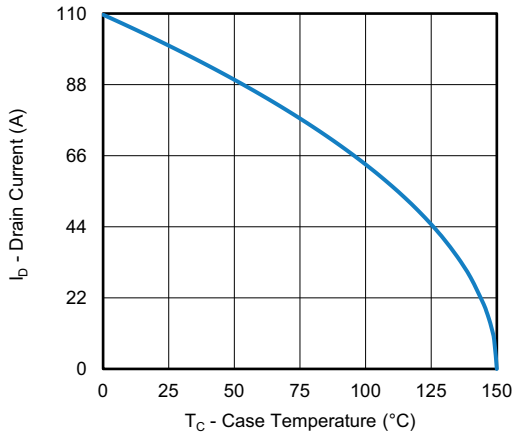
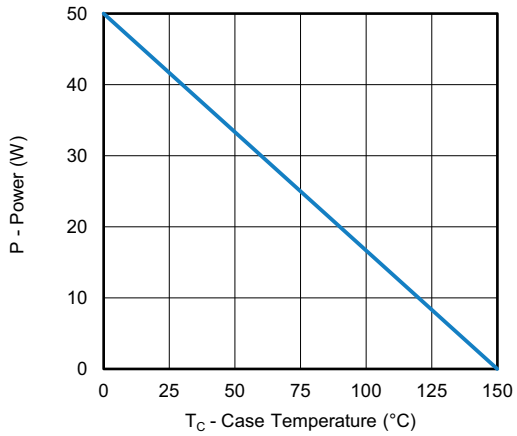


Current Derating [a]



Power, Junction-to-Case

Notes

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

b. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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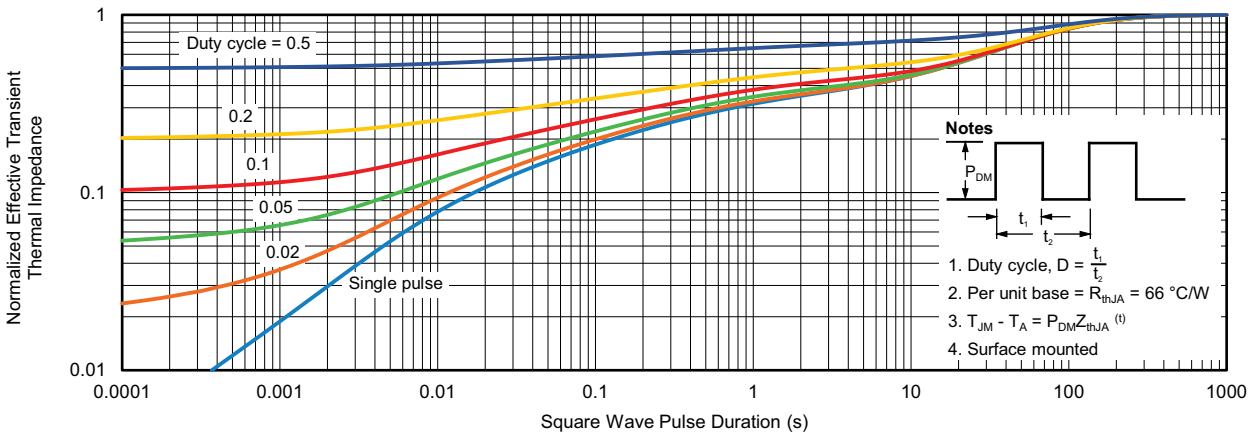
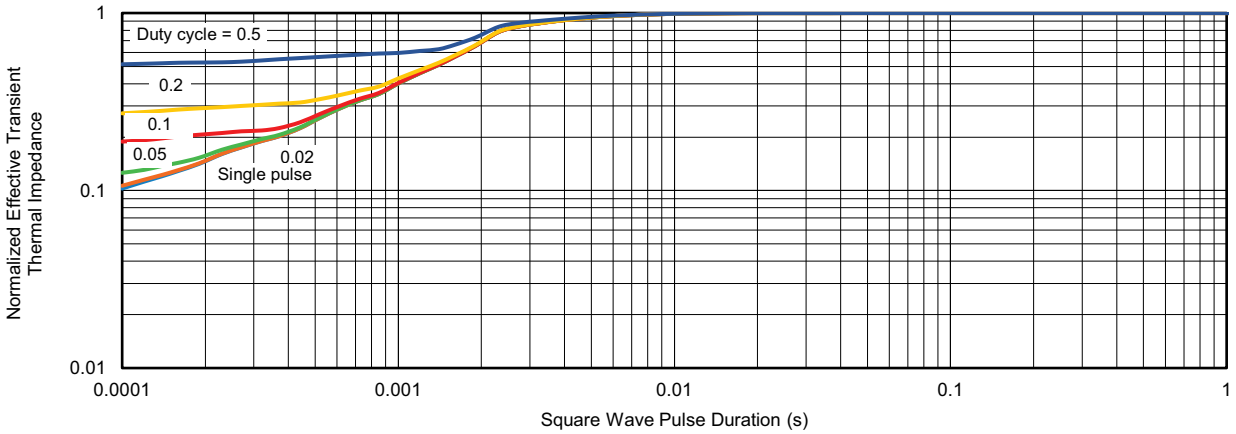


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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